

**FEATURES**

- Quadrature VCO Outputs
- Wide Frequency Range (0.01Hz to 300kHz)
- Wide Supply Voltage Range (4.5V to 20V)
- TTL/HCMOS Compatible ( $V_{CC} = 5VDC$ )
- Wide Dynamic Range (2mV to 3Vrms)
- Adjustable Tracking Range ( $\pm 1\%$  to  $\pm 80\%$ )
- Excellent Temp. Stability 20ppm/°C, Typ.

**APPLICATIONS**

- Frequency Synthesis
- Data Synchronization
- FM Detection
- Tracking Filters
- FSK Demodulation

**GENERAL DESCRIPTION**

The XR-2212 is an ultra-stable monolithic phase-locked loop (PLL) system especially designed for data communications and control system applications. Its on board reference and uncommitted operational amplifier, together with a typical temperature stability of better than 20ppm/°C, make it ideally suited for frequency synthesis,

FM detection, and tracking filter applications. The wide input dynamic range, large operating voltage range, large frequency range, and HCMOS and TTL compatibility contribute to the usefulness and wide applicability of this device.

**ORDERING INFORMATION**

Part No.	Package	Operating Temperature Range
XR-2212M	16 Lead 300 Mil CDIP	-55°C to +125°C
XR-2212CP	16 Lead 300 Mil PDIP	0°C to +70°C

**BLOCK DIAGRAM**

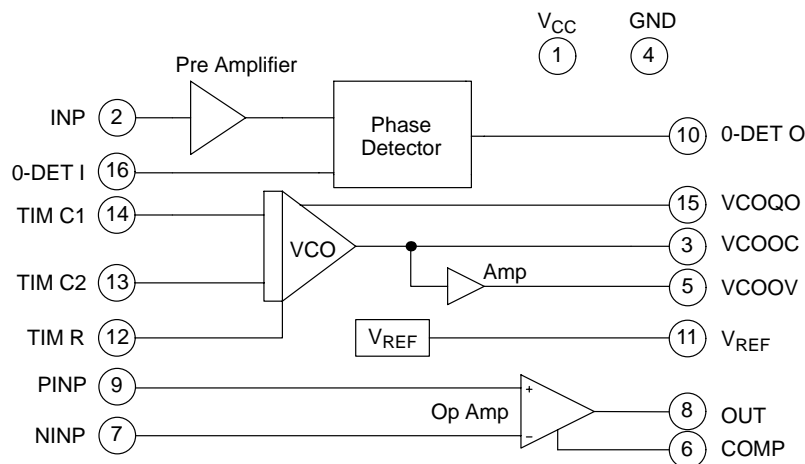
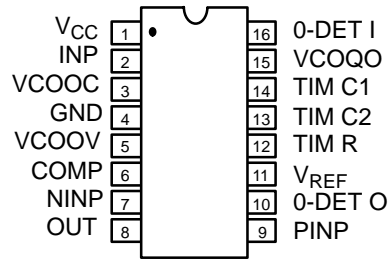


Figure 1. XR-2212 Block Diagram

## PIN CONFIGURATION



16 Lead PDIP, CDIP (0.300")

## PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	V <sub>CC</sub>		<b>Positive Power Supply.</b>
2	INP	I	<b>Receive Analog Input.</b>
3	VCOOC	O	<b>VCO Current Output.</b>
4	GND		<b>Ground Pin.</b>
5	VCOOV	O	<b>VCO Voltage Source Output.</b>
6	COMP	I	<b>Uncommitted Amplifier, Frequency Compensation Input.</b>
7	NINP	I	<b>Inverted Input.</b> Uncommitted amplifier.
8	OUT	O	<b>Uncommitted Amplifier Output.</b>
9	PINP	I	<b>Positive Input.</b> Uncommitted amplifier.
10	0-DET O	O	<b>Phase Detector Output.</b>
11	V <sub>REF</sub>	O	<b>Internal Voltage Reference.</b> The value of V <sub>REF</sub> is V <sub>CC</sub> /2 -650mV.
12	TIM R	I	<b>Timing Resistor Input.</b> This pin connects to the timing resistor of the VCO.
13	TIM C2	I	<b>Timing Capacitor Input.</b> The timing capacitor connects between this pin and pin 14.
14	TIM C1	I	<b>Timing Capacitor Input.</b> The timing capacitor connects between this pin and pin 13.
15	VCOQO	O	<b>VCO Quadrature Output.</b>
16	0-DET I	I	<b>Phase Detector Input.</b>

## ELECTRICAL CHARACTERISTICS

Test Conditions:  $V_{CC} = +12V$ ,  $T_A = +25^\circ C$ ,  $R_0 = 30k\Omega$ ,  $C_0 = 0.033\mu F$ , unless otherwise specified. See *Figure 3* for component designation.

Parameter	XR-2212M			XR-2212CP			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>General Characteristics</b>								
Supply Voltage	4.5		<b>15</b>	4.5		<b>15</b>	V	
Supply Current		6	<b>10</b>		6	<b>12</b>	mA	$R_0 \geq 10k\Omega$ , See <i>Figure 5</i>
<b>Oscillator Section</b>								
Frequency Accuracy		$\pm 1$	<b><math>\pm 3</math></b>		$\pm 1$		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability								$R_1 = \infty$
Temperature		$\pm 20$	$\pm 50$		$\pm 20$		ppm/ $^\circ C$	See <i>Figure 9</i>
Power Supply		0.05	<b>0.5</b>		0.05		%/V	$V_{CC} = 12 \pm 1V$ , See <i>Figure 8</i>
		0.2			0.2		%/V	$V_{CC} = 5 \pm 0.5V$ , See <i>Figure 8</i>
Upper Frequency Limit	<b>100</b>	300			300		kHz	$R_0 = 8.2k\Omega$ , $C_0 = 400pF$
Lowest Practical Operating Frequency			0.01		0.01		Hz	$R_0 = 2M\Omega$ , $C_0 = 50\mu F$
Timing Resistor, $R_0$								See <i>Figure 5</i>
Operating Range	5		2000	5		2000	k $\Omega$	
Recommended Range	15		100	15		100	k $\Omega$	See <i>Figure 8</i> and <i>Figure 9</i>
<b>Oscillator Outputs</b>								
Voltage Output								Measured at Pin 5
Positive Swing, $V_{OH}$		11			11		V	
Negative Swing, $V_{OL}$		0.4	<b>0.8</b>		0.5		V	
Current Sink Capability		1			1		mA	
Current Output								Measured at Pin 3
Peak Current Swing	<b>100</b>	150			150		$\mu A$	
Output Impedance		1			1		M $\Omega$	
Quadrature Output								Measured at Pin 15
Output Swing		0.6			0.6		V	
DC Level		0.3			0.3		V	Referenced to Pin 11
Output Impedance		3			3		k $\Omega$	
<b>Loop Phase Detector Section</b>								<b>Measured at Pin 10</b>
Peak Output Current	<b><math>\pm 150</math></b>	$\pm 200$	<b><math>\pm 300</math></b>	<b><math>\pm 100</math></b>	$\pm 200$	<b><math>\pm 300</math></b>	$\mu A$	
Output Offset Current		$\pm 1$			$\pm 2$		$\mu A$	
Output Impedance		1			1		M $\Omega$	
Maximum Swing	<b><math>\pm 4</math></b>	$\pm 5$		<b><math>\pm 4</math></b>	$\pm 5$		V	Referenced to Pin 11

### Note

**Bold face parameters** are covered by production test and guaranteed over operating temperature range.

## ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	XR-2212M			XR-2212CP			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>Input Preamp Section</b>								Measured at Pin 2
Input Impedance		20			20		kΩ	
Input Signal to Cause Limiting		2	10		2		mV rms	
<b>Op Amp Section</b>								
Voltage Gain	<b>55</b>	70		55	70		dB	$R_L = 5.1k\Omega, R_F = \infty$
Input Bias Current		0.1	<b>1</b>		0.1	<b>1</b>	μA	
Offset Voltage		±5	<b>±20</b>		±5	<b>±20</b>	mV	
Slew Rate		2			2		V/μsec	
<b>Internal Reference</b>								Measured at Pin 11
Voltage Level	<b>4.9</b>	5.3	<b>5.7</b>	<b>4.75</b>	5.3	<b>5.85</b>	V	AC Small Signal
Output Impedance		100			100		Ω	
Maximum Source Current		80			80		ΩA	

### Note

**Bold face parameters** are covered by production test and guaranteed over operating temperature range.

Specifications are subject to change without notice

## ABSOLUTE MAXIMUM RATINGS

Power Supply ..... 18V  
 Input Signal Level ..... 3V rms

Power Dissipation:  
 Ceramic Package: ..... 750mW  
 Derate Above  $T_A = +25^\circ\text{C}$  ..... 6mW/°C  
 Plastic Package: ..... 625mW  
 Derate Above  $T_A = +25^\circ\text{C}$  ..... 5mW/°C

## SYSTEM DESCRIPTION

The XR-2212 is a complete PLL system with buffered inputs and outputs, an internal reference, and an uncommitted op amp. Two VCO outputs are pinned out; one sources current, the other sources voltage. This enables operation as a frequency synthesizer using an external programmable divider. The op amp section can be used as an audio preamplifier for FM detection or as a high speed sense amplifier (comparator) for FSK demodulation. The center frequency, bandwidth, and tracking range of the PLL are controlled independently by

external components. The PLL output is directly compatible with CMOS, HCMOS and TTL logic families as well as microprocessor peripheral systems.

The precision PLL system operates over a supply voltage range of 4.5V to 20V, a frequency range of 0.01Hz to 300kHz, and accepts input signals in the range of 2mV to 3V rms. Temperature stability of the VCO is typically better than 20 ppm/°C with the optimum timing resistor value.



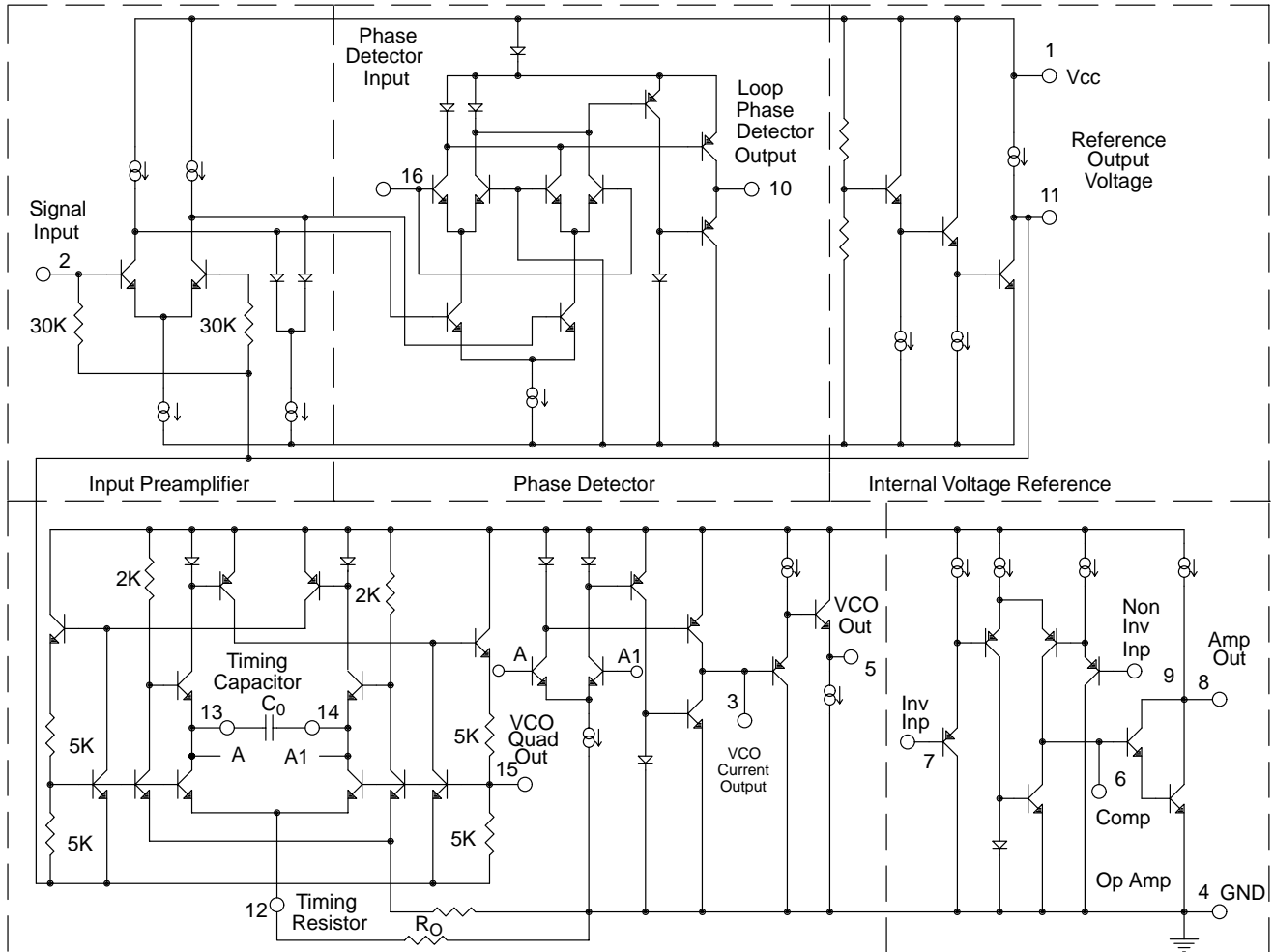
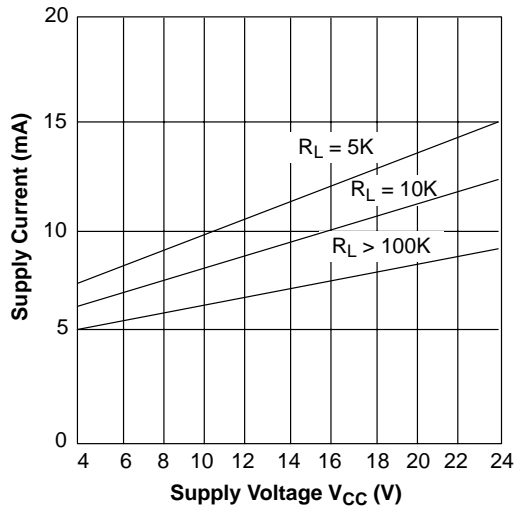
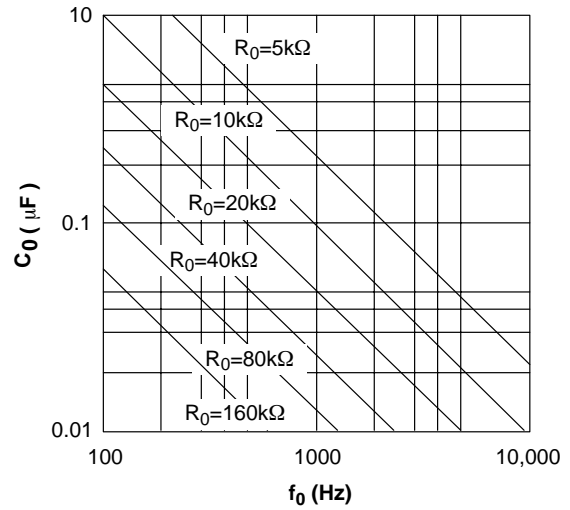


Figure 4. Simplified Circuit Schematic of XR-2212

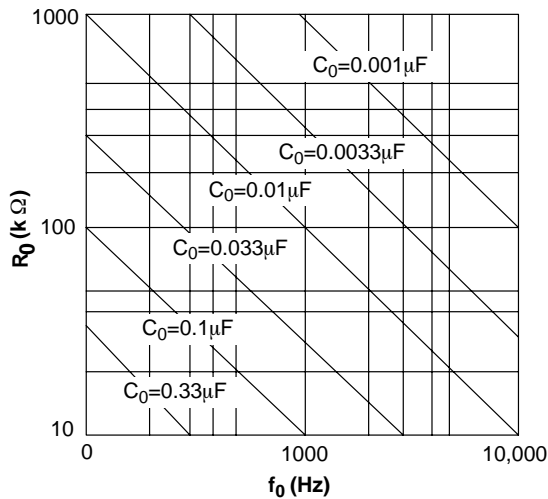
**TYPICAL CHARACTERISTICS**



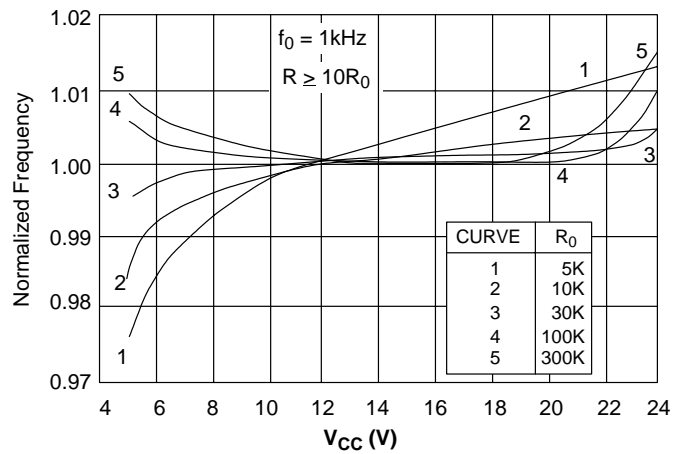
**Figure 5. Typical Supply Current vs. V<sub>CC</sub> (Logic Outputs Open Circuited)**



**Figure 6. VCO Frequency vs. Timing Resistor**



**Figure 7. VCO Frequency vs. Timing Capacitor**



**Figure 8. Typical f<sub>0</sub> vs. Power Supply Characteristics**

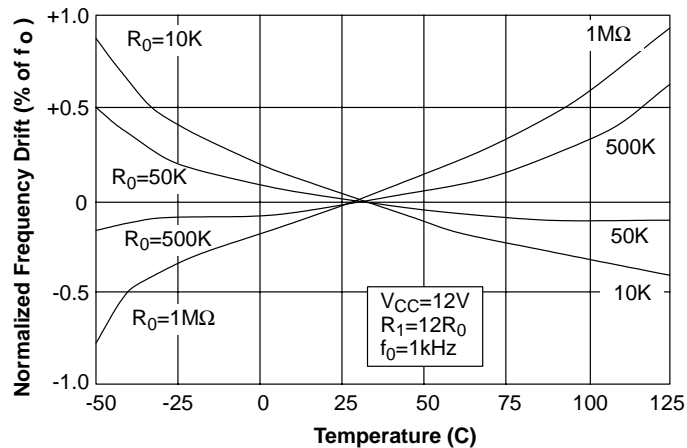


Figure 9. Typical Center Frequency Drift vs. Temperature

## DESCRIPTION OF CIRCUIT CONTROLS

**Signal Input (Pin 2):** Signal is AC coupled to this terminal. The internal impedance at Pin 2 is 20kΩ. Recommended input signal level is in the range of 10mV to 5V peak-to-peak.

**VCO Current Output (Pin 3):** This is a high impedance (MΩ) current output terminal which can provide  $\pm 100\mu\text{A}$  drive capability with a voltage swing equal to  $V_{CC}$ . This output can directly interface with CMOS or NMOS logic families.

**VCO Voltage Output (Pin 5):** This terminal provides a low-impedance ( $\approx 50\Omega$ ) buffered output for the VCO. It can directly interface with low-power Schottley TTL. For interfacing with standard TTL circuits, a 750Ω pull-down resistor from Pin 5 to ground is required. For operation of the PLL without an external divider, Pin 5 can be DC coupled to Pin 16.

**Op Amp Compensation (Pin 6):** The op amp section is frequency compensated by connecting an external capacitor from Pin 6 to the amplifier output (Pin 8). For unity-gain compensation a 20pF capacitor is recommended.

**Op Amp Inputs (Pins 7 and 9):** These are the inverting and the non-inverting inputs for the op amp section. The common-mode range of the op amp inputs is from +1V to  $(V_{CC} - 1.5)$  volts.

**Op Amp Output (Pin 8):** The op amp output is an open-collector type gain stage and requires a pull-up resistor,  $R_L$ , to  $V_{CC}$  for proper operation. For most applications, the recommended value of  $R_L$  is in 5kΩ to 10kΩ range.

**Phase Detector Output (Pin 10):** This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by  $R_1$  and  $C_1$  connected to Pin 10 (see Figure 3). With no input signal, or with no phase-error within the PLL, the DC level at Pin 10 is very nearly equal to  $V_{REF}$ . The peak voltage swing available at the phase detector output is equal to  $\pm V_{REF}$ .

**Reference Voltage,  $V_{REF}$  (Pin 11):** This pin is internally biased at the reference voltage level.  $V_{REF}: V_{REF} = V_{CC}/2 - 650\text{mV}$ . The DC voltage level at this pin forms an internal reference for the voltage levels at Pins 10, 12 and 16. Pin 11 must be bypassed to ground with a 0.1μF capacitor, for proper operation of the circuit.

**VCO Control Input (Pin 12):** VCO free-running frequencies determined by external timing resistor,  $R_0$ , connected from this terminal to ground. For optimum temperature stability,  $R_0$  must be in the range of 10kΩ to 100kΩ (see Figure 9).

**VCO Frequency Adjustment:** VCO can be fine-tuned by connecting a potentiometer,  $R_X$ , in series with  $R_0$  at Pin 12 (see Figure 11).

This terminal is a low-impedance point, and is internally biased at a DC level equal to  $V_{REF}$ . The maximum timing



current drawn from Pin 12 must be limited to  $\leq 3$  mA for proper operation of the circuit.

**VCO Timing Capacitor** (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor,  $C_0$ , connected across these terminals (see *Figure 6*).  $C_0$  must be nonpolar, and in the range of 200pF to 10 $\mu$ F.

**VCO Quadrature Output** (Pin 15): The low-level ( $\approx 0.6$ Vpp) output at this pin is at quadrature phase (i.e. 90° phase-offset) with the other VCO outputs at Pins 3 and 5. The DC level at Pin 15 is approximately 300mV above  $V_{REF}$ . The quadrature output can be used with an external multiplier as a “lock detect” circuit. In order not to degrade oscillator performance, the output at Pin 15 must be buffered with an external high impedance low capacitance amplifier. When not in use, Pin 15 should be left open-circuited.

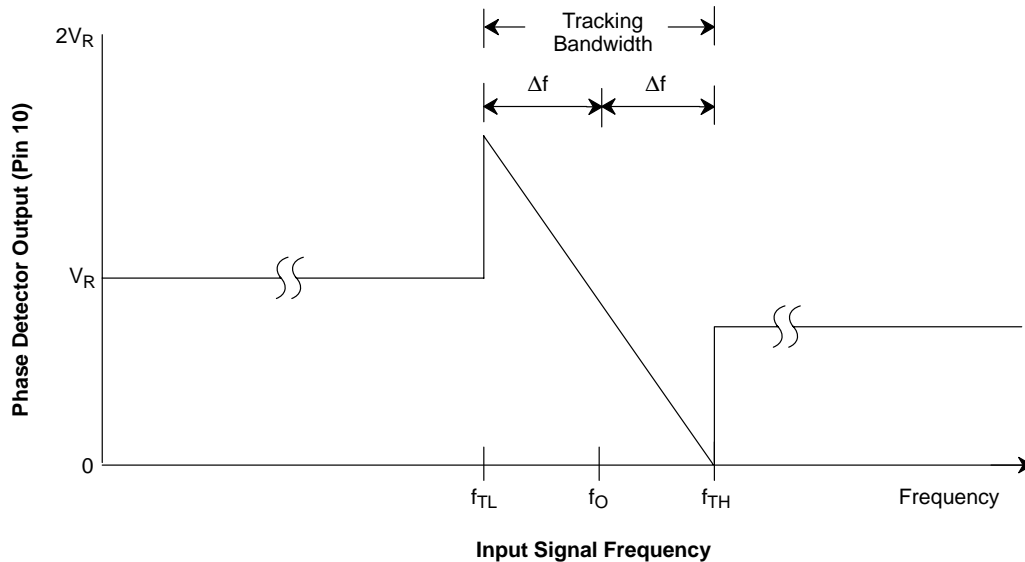
**Phase Detector Input** (Pin 16): Voltage output of the VCO (Pin 5) or the output of an external frequency divider

is connected to this pin. The DC level of the sensing threshold for the phase detector is referenced to  $V_{REF}$ . If the signal is capacitively coupled to Pin 16, then this pin must be biased from Pin 11, through an external resistor,  $R_B$  ( $R_B \approx 10$ k $\Omega$ ). The peak voltage swing applied to Pin 16 must not exceed ( $V_{CC} - 1.5$ ) volts.

**PHASE-LOCKED LOOP PARAMETERS**

**Transfer Characteristics**

*Figure 10* shows the basic frequency to voltage characteristics of XR-2212. With no input signal present, filtered phase detector output voltage is approximately equal to the internal reference voltage,  $V_{REF}$  at Pin 11. The PLL can track an input signal over its tracking bandwidth, shown in the figure. The frequencies  $f_{TL}$  and  $f_{TH}$  represent the lower and the upper edge of the tracking range,  $f_0$  represents the VCO center frequency.



**Figure 10. Phase Detector Output Voltage (Pin 10) as a Function of Input Signal Frequency**

**Note**

Output Voltage is Referenced to Internal Reference Voltage  $V_{REF}$  at Pin 11

**Design Equations**

(See *Figure 3* and *Figure 10* for definition of components.)

1. VCO Center Frequency,  $f_0$ :  $f_0 = 1/R_0C_0$  Hz
2. Internal Reference Voltage,  $V_{REF}$  (measured at Pin 11)  
 $V_{REF} = V_{CC}/2 - 650\text{mV}$
3. Loop Low-Pass Filter Time Constant,  $\tau$ :  $\tau = R_1C_1$
4. Loop Damping,  $\zeta$ :

$$\zeta = 0.25 \sqrt{\frac{NC_0}{C_1}}$$

where N is the external frequency divider modular (See 2). If no divider is used,  $N = 1$ .

5. Loop Tracking Bandwidth,  $\pm \Delta f/f_0$ :  $\Delta f/f_0 = R_0/R_1$
6. Phase Detector Conversion Gain,  $K_\theta$ : ( $K_\theta$  is the differential DC voltage across Pins 10 and 11, per unit of phase error at phase-detector input)  
 $K_\theta = -2V_{REF}/\pi$  volts/radian
7. VCO Conversion Gain,  $K_0$ : ( $K_0$  is the amount of change in VCO frequency, per unit of DC voltage change at Pin 10. It is the reciprocal of the slope of conversion characteristics shown in *Figure 10*).  
 $K_0 = -1/V_{REF}C_0R_1$  Hz/V
8. Total Loop Gain,  $K_T$   
 $K_T = 2\pi K_\theta K_0 = 4/C_0R_1$  rad/sec/volt
9. Peak Phase-Detector Current,  $I_A$ ; available at Pin 10.  
 $I_A = V_{REF}(\text{volts})/25\text{mA}$

**APPLICATION INFORMATION****FM Demodulation**

XR-2212 can be used as a linear FM demodulator for both narrow-band and wide-band FM signals. The generalized circuit connection for this application is shown in *Figure 11*, where the VCO output (Pin 5) is directly connected to the phase detector input (Pin 16). The demodulated signal is obtained at phase detector output (Pin 10). In the circuit connection of *Figure 10*, the op amp section of XR-2212 is used as a buffer amplifier to provide both additional voltage amplification as well as current drive capability. Thus, the demodulated output signal available at the op amp output (Pin 8) is fully buffered from the rest of the circuit.

In the circuit of *Figure 11*,  $R_0C_0$  set the VCO center frequency,  $R_1$  sets the tracking bandwidth,  $C_1$  sets the low-pass filter time constant. Op amp feedback resistors  $R_F$  and  $R_C$  set the voltage gain of the amplifier section.

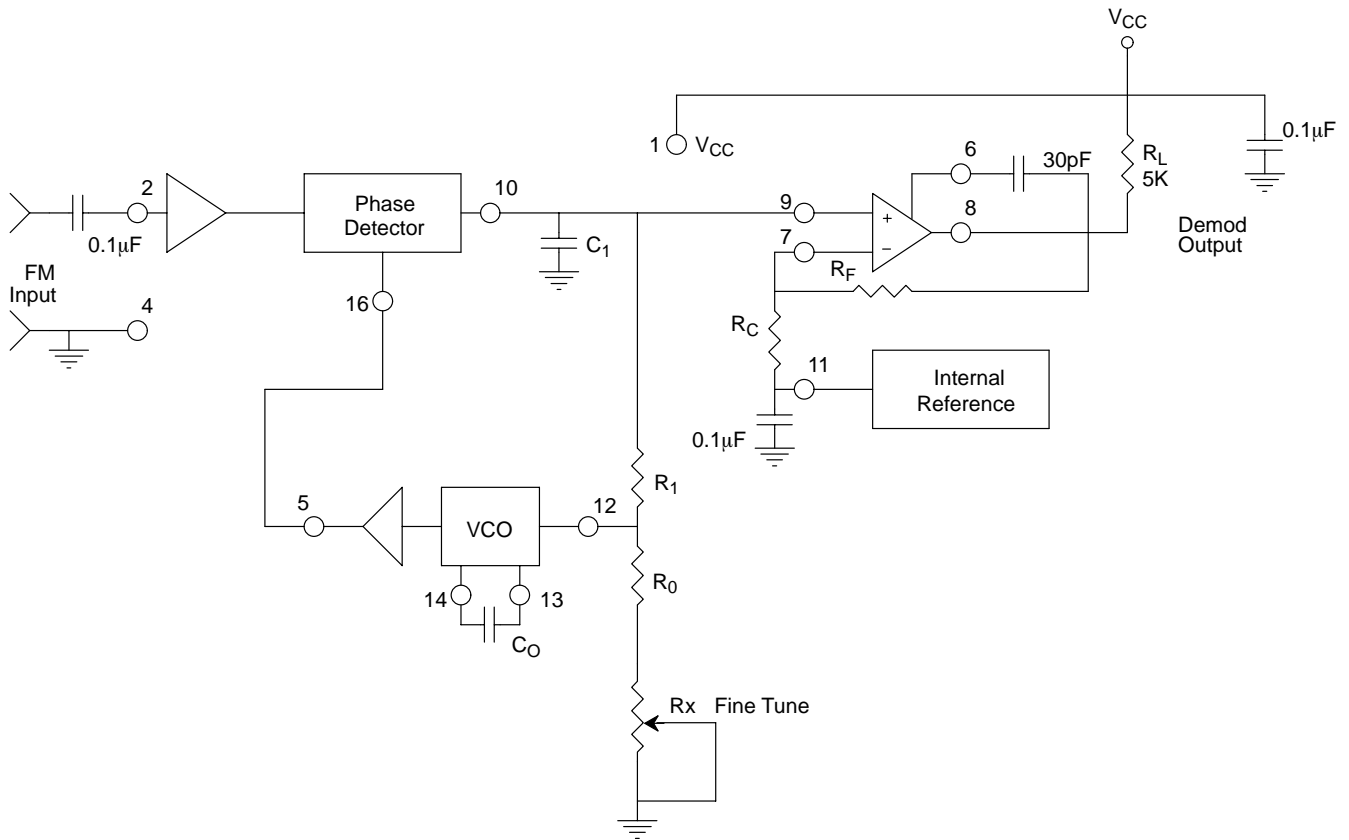


Figure 11. Circuit Connection for FM Demodulation

**Design Instructions**

The circuit of *Figure 11* can be tailored to any FM demodulation application by a choice of the external components  $R_0$ ,  $R_1$ ,  $R_C$ ,  $R_F$ ,  $C_0$  and  $C_1$ . For a given FM center frequency and frequency deviation, the choice of these components can be calculated as follows, using the design equations and definitions given on page 10.

- a) Choose VCO center frequency  $f_0$  to be the same as FM carrier frequency.
- b) Choose value of timing resistor  $R_0$ , to be in the range of 10kΩ to 100kΩ. This choice is arbitrary. The recommended value is  $R_0 = \sim 20k\Omega$ . The final value of  $R_0$  is normally fine-tuned with the series potentiometer,  $R_X$ .
- c) Calculate value of  $C_0$  from design equation (1) or from *Figure 7*:

$$C_0 = 1/R_0f_0$$

- d) Choose  $R_1$  to determine the tracking bandwidth,  $\Delta f$  (see design equation 5). The tracking bandwidth,  $\Delta f$ , should be set significantly wider than the maximum input FM signal deviation,  $\Delta f_{SM}$ . Assuming the tracking bandwidth to be “N” times larger than  $\Delta f_{SM}$ , one can re-unite design equation 5 as:

$$\frac{\Delta f}{f_0} = \frac{R_0}{R_1} = N \frac{\Delta f_{SM}}{f_0}$$

*Table 2.* lists recommended values of N, for various values of the maximum deviation of the input FM signal.

- e) Calculate  $C_1$  to set loop damping (see design equation 4). Normally,  $\zeta = 1/2$  is recommended. Then,  $C_1 = C_0/4$  for  $\zeta = 1/2$ .

% Deviation of FM Signal ( $\Delta f_{SM}/f_0$ )	Recommended Value of Bandwidth Ratio, N ( $N = \Delta f/\Delta f_{SM}$ )
1% or less	10
1% to 3%	5
1% to 5%	4
5% to 10%	3
10% to 30%	2
30% to 50%	1.5

**Table 2.**

Recommended values of bandwidth ratio, N, for various values of FM signal frequency deviation. (Note: N is the ratio of tracking bandwidth  $\Delta f$  to max. signal frequency deviation,  $\Delta f_{SM}$ ).

- f) Calculate  $R_C$  and  $R_F$  to set peak output signal amplitude. Output signal amplitude,  $V_{OUT}$ , is given as:

$$V_{OUT} = \left(\frac{\Delta f_{SM}}{f_0}\right)(V_{REF})\left(\frac{R_1}{R_0}\right)\left(\frac{R_C + R_F}{R_C}\right)$$

In most applications,  $R_F = 100k\Omega$  is recommended; then  $R_C$ , can be calculated from the above equation to give desired output swing. The output amplifier can also be used as a unity-gain voltage follower, by open circuiting  $R_C$  (i.e.,  $R_C = \infty$ ).

**Note:** All calculated component values except  $R_0$  can be rounded-off to the nearest standard value, and  $R_0$  can be varied to fine-tune center frequency, through a series potentiometer,  $R_X$ , (See Figure 11).

### Design Example

Demodulator for FM signal with 67kHz carrier frequency with  $\pm 5$ kHz frequency deviation. Supply voltage is +12V and required peak output swing is  $\pm 4$ V.

- Step a)  $f_0$  is chosen as 67kHz.  
 Step b) Choose  $R_0 = 20k\Omega$  (18k $\Omega$  fixed resistor in series with 5k $\Omega$  potentiometer).  
 Step c) Calculate  $C_0$ ; from design equation (1).  
 $C_0 = 746pF$   
 Step d) Calculate  $R_1$ . For given FM deviation,  $\Delta f_{SM}/f_0 = 0.0746$ , and  $N = 3$  from Table 2. Then:

$$R_0/R_1 = (3)(0.0746) = 0.224$$

or:

$$R_1 = 89.3k\Omega.$$

Step e): Calculate  $C_1 = (C_0/4) = 186pF$ .

Step f): Calculate  $R_C$  and  $R_F$  to get  $\pm 4$ V peak output swing: Let  $R_F = 100k\Omega$ . Then,

$$R_C = 80.6k\Omega.$$

**Note:** All values except  $R_0$  can be rounded-off to nearest standard value.

### FREQUENCY SYNTHESIS

Figure 12 shows the generalized circuit connection for frequency synthesis. In this application an external frequency divider is connected between the VCO output (Pin 5) and the phase-detector input (Pin 16). When the circuit is in lock, the two signals going into the phase-detector are at the same frequency, or  $f_S = f_1/N$  where N is the modulus of the external frequency divider. Conversely, the VCO output frequency,  $f_1$  is equal to  $Nf_S$ .

In the circuit configuration of Figure 12, the external timing components,  $R_0$  and  $C_0$ , set the VCO free running frequency;  $R_1$  sets the tracking bandwidth and  $C_1$  sets the loop damping, i.e., the low-pass filter time constant (see design equations).

The total tracking range of the PLL (see Figure 10), should be chosen to accommodate the lowest and the highest frequency,  $f_{max}$  and  $f_{min}$ , to be synthesized. A recommended choice for most applications is to choose a tracking half-bandwidth  $\Delta f$ , such that:

$$\Delta f \approx f_{max} - f_{min}$$

If a variable input frequency and a variable counter modulus N is used, then the maximum and the minimum values of output frequency will be:

$$f_{max} = N_{max}(f_S)_{max} \text{ and } f_{min} = N_{min}(f_S)_{min}$$

If a fixed output frequency is desired, i.e. N and  $f_S$  are fixed, then a  $\pm 10\%$  tracking bandwidth is recommended. Excessively large tracking bandwidth may cause the PLL to lock on the harmonics of the input signals; and the small tracking range increases the "lock-up" or acquisition time.

### Design Instructions

For a given performance requirement, the circuit of Figure 12 can be optimized as follows:

- a) Choose center frequency,  $f_0$ , to be equal to the output frequency to be synthesized. If a range of output

frequencies is desired, set  $f_0$  to be at mid-point of the desired range.

- b) Choose timing resistor  $R_0$  to be in the range of 15k $\Omega$  to 100k $\Omega$ . This choice is arbitrary.  $R_0$  can be fine tuned with a series potentiometer,  $R_x$ .
- c) Choose timing capacitor,  $C_0$  from *Figure 7* or Equation 1.
- d) Calculate  $R_1$  to set tracking bandwidth (see *Figure 10* and design equation 5). If a range of output frequencies are desired, set  $R_1$  to get:

$$\Delta f = f_{max} - f_{min}$$

If a single fixed output frequency is desired, set  $R_1$  to get:

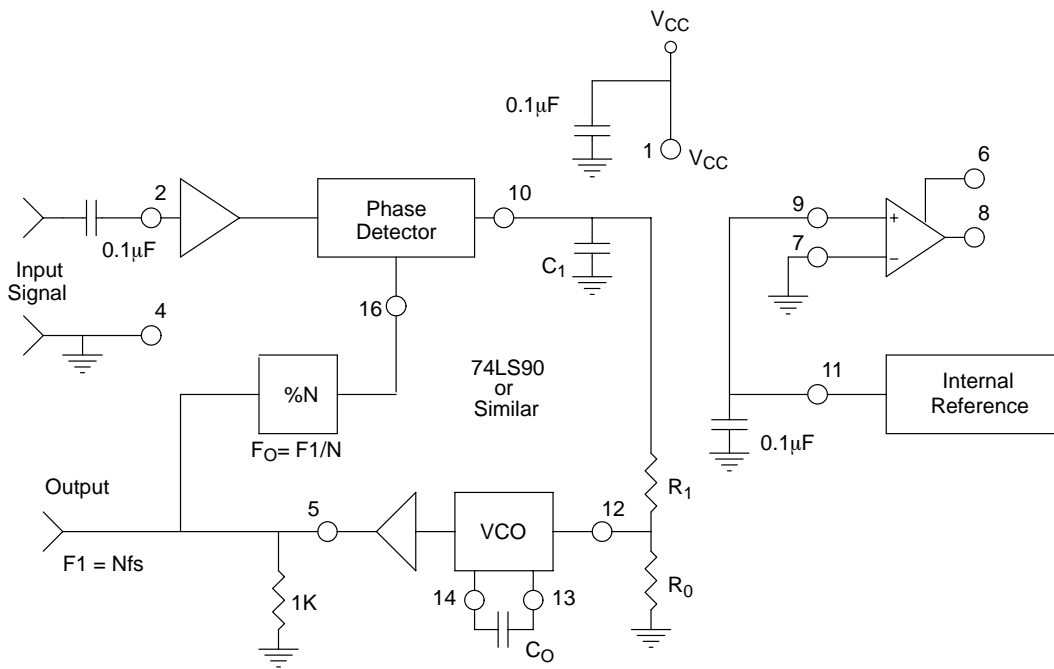
$$\Delta f = 0.1 f_0$$

- e) Calculate  $C_1$  to obtain desired loop damping. (See design equation 4). For most applications,  $\zeta = 1/2$  is recommended, thus:

$$C_0 = NC_0/4$$

**Note**

All component values except  $R_0$  can be rounded off to the nearest standard value.



**Figure 12. Circuit Connection for Frequency Synthesizer**

## INPUT SENSITIVITY

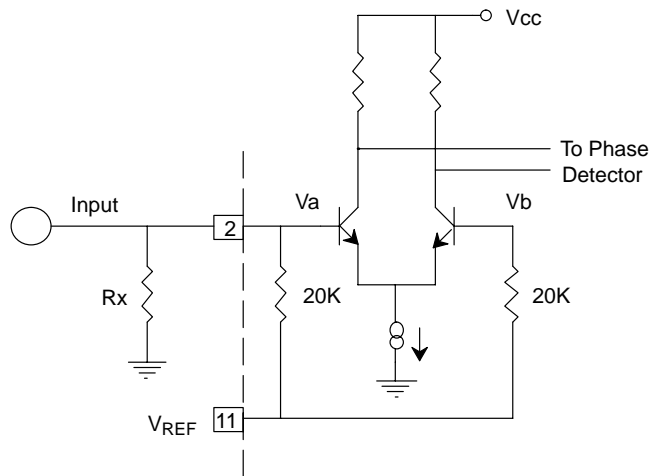
The input to the XR-2212 may sometimes be too sensitive to noise conditions on the input line. *Figure 13* illustrates a method of de-sensitizing the XR-2212 from such noisy line conditions by the use of a resistor,  $R_x$ , connected from pin 2 to ground. The value of  $R_x$  is chosen by the equation and the desired minimum signal threshold level.

$V_{IN}$  minimum (peak) input voltage must exceed this value to be detected (equivalent to adjusting  $V$  threshold).

$$V_{IN} \text{ minimum (peak)} = V_a - V_b =$$

$$\Delta V \pm 2.8V \text{ offset} = V_{REF} = \frac{20,000}{(20,000 + R_x)} \text{ or}$$

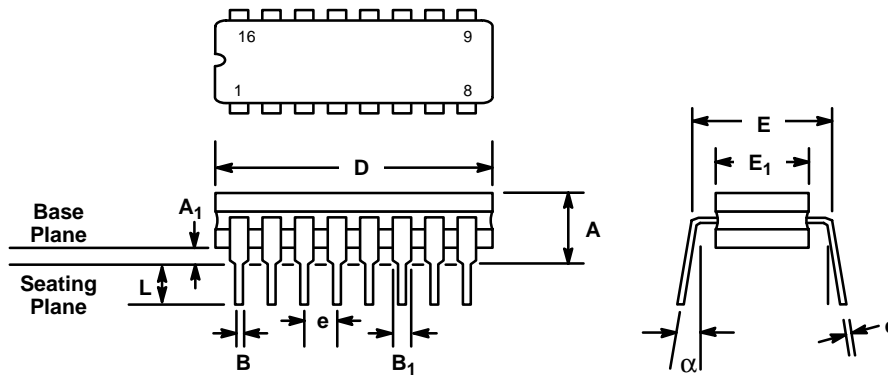
$$R_x = 20,000 \left( \frac{V_{REF}}{\Delta V} - 1 \right)$$



**Figure 13. Desensitizing Input Stage**

**16 LEAD CERAMIC DUAL-IN-LINE  
(300 MIL CDIP)**

*Rev. 1.00*

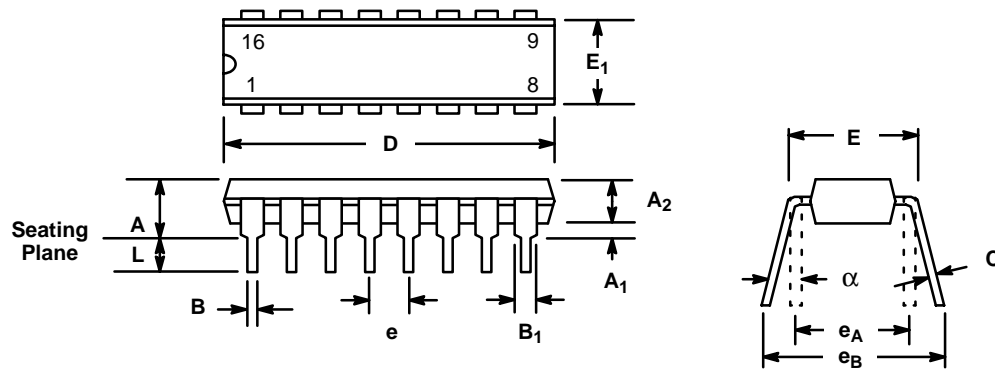


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A <sub>1</sub>	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B <sub>1</sub>	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.740	0.840	18.80	21.34
E <sub>1</sub>	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

*Note: The control dimension is the inch column*

## 16 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A <sub>1</sub>	0.015	0.070	0.38	1.78
A <sub>2</sub>	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B <sub>1</sub>	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E <sub>1</sub>	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e <sub>A</sub>	0.300 BSC		7.62 BSC	
e <sub>B</sub>	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column



**Notes**

**Notes**

**Notes**

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